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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,222	07/03/2003	Masatoshi Akagawa	300.1119	5751
21171	7590	03/08/2007		
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER CHANG, RICK KILTAE	
			ART UNIT 3726	PAPER NUMBER
			MAIL DATE 03/08/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

SP

**Advisory Action
Before the Filing of an Appeal Brief**

Application No.

10/612,222

Applicant(s)

AKAGAWA ET AL.

Examiner

Rick K. Chang

Art Unit

3726

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 14 February 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).


4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: see final Office Action.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.


RICHARD CHANG
PRIMARY EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: The examiner maintains his rejections. Means plus function language used in claim 49 is referring to an apparatus, while claim 1 'ing language is referring to steps. Therefore, they are different inventions. Leedy discloses that "the data resulting from the tester signal process is a list of the location of each defective transistors or ICLUs" (col. 5, lines 33-35). This anticipates the detecting step in claim 1, lines 4-5. Then, Leedy discloses "this list is automatically communicated to the conventional CAD means from the tester tester signal processor. the CAD means then, by special software algorithms works out an interconnect strategy for each die" (col. 5, lines 35-39). This anticipates that the software calculates a displacement between the design position of the first electronic component and the actual position of the first electronic component on the surface of the board, and holding the displacement as first displacement data (the software is installed in a hard drive of a computer, which stores all data regarding the wafer). Thereafter, Leedy discloses "the master placement scheme of the net list is modified in terms of the placement of the defective ICLUs so as to bypass the defective ICLUs and interconnect defect-free ICLUs from the stock of redundant ICLUs" (col. 5, lines 39-43). This anticipates correcting design data to be used for processing the board. Col. 6, lines 45-47 discloses that the modified net list is next used to produce the database for the desired interconnect patterns on the wafer using E-beam means. Subsequently, depositing a layer of insulation over the wafer surface, then a layer of metal is deposited over the insulation layer (col. 6, lines 47-58).